

[54] SYMMETRICAL INPUT NOR/NAND GATE CIRCUIT

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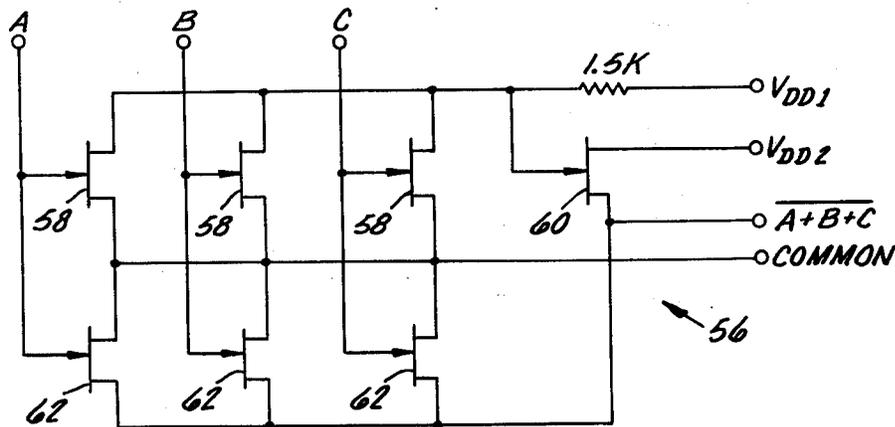
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[57] ABSTRACT

An electrical circuit is shown having first and second pluralities of junction field effect transistors connected with an output transistor to provide NOR/NAND gate logic operation. The junction field effect transistors are preferably enhancement mode junction field effect transistors selected so that the circuit can be constructed as described on an integrated circuit chip.

5 Claims, 5 Drawing Figures



$$Z_L = 10.5 \text{ pF} + 1 \text{ K}$$

$$P_D = 2.6 \text{ mW (ON)}, 100 \text{ } \mu\text{W (OFF)}$$

$$t_{pd} = 3 \text{ ns}$$

$$P_{D(ON)} \times t_{pd} = 4 \text{ pJ (50% ON-OFF)}$$